REMARKS

Applicant submits that the present application, as currently amended, is in condition for allowance.

Claims 66-78 and 80-129 are pending, with claims 66, 82, 94, 97, 101, 122 and 127 amended, and claims 79 and 130 cancelled without prejudice or disclaimer, by the present amendment.

In the Official Action, claims 66-84 and 97-130 were rejected under 35 U.S.C. § 101; claims 66-130 were rejected under 35 U.S.C. § 102(b) as being anticipated by Dalton (WO 01/01298); and claims 66-68 and 101-103 were rejected under 35 U.S.C. § 103(a) in view of Dalton and Examiner's Official Notice.

Claims 66, 94, 101 and 127 are amended to more clearly describe and distinctly claim Applicant's invention. In particular, the features of previously examined claim 79 have been incorporated into independent claim 66. Claims 82 and 94 have been amended to correct a typographical error. No new matter is added.

Briefly recapitulating, amended claim 66 is directed to a parallel processing method of logic event simulation on circuits comprising a plurality of logic gates, the method including, *inter alia*, the following features:

> for a time period, identifying segments that have a state S0 in that time period based on the segment data stored in the circuit segment table;
>
> bringing only the segments with a state S0, one at a time, into the associative memory mechanism from external memory for evaluation; and
>
> evaluating the segments with a state S0 in the associative memory mechanism and storing a result of the evaluation in a tangible medium.

Thus, Applicant submits that claim 66 recites a variety of useful and tangible results (e.g., bringing segments into memory; evaluating; and storing an evaluation result). Independent claim 101 is similarly amended. Therefore, Applicant submits that the rejections under 35 U.S.C. § 101 is moot.

More specifically, the applicant strongly disagrees with the Examiners assertion that WO01/01298 (Dalton) discloses a method or processor in which the circuit is divided into a plurality of circuit segments which are stored in external memory. The Examiner has equated this feature with partitioning of a circuit (a technique not described previously with associated memory mechanisms). Partitioning requires multiple processors used in parallel to simulate the circuit. Previously,

Dalton discloses a method in which an entire circuit is brought into the associative memory mechanism at the same time. However, Dalton does not disclose or suggest

> ***dividing the circuit representation into a plurality of circuit segments***, at least one of the circuit segments containing a plurality of logic gates;
>
> ***assigning a unique segment identifier to each segment;***
>
> generating a circuit segment table in the associative memory and storing the unique segment identifiers along with segment data in a circuit segment table;
>
> for a time period, identifying segments that have a state S0 in that time period based on the segment data stored in the circuit segment table;
>
> ***bringing only the segments with a state S0, one at a time***, into the associative memory mechanism from external memory for evaluation; and
>
> evaluating segments with a state S0, in the associative memory mechanism and storing a result of the evaluation in a tangible medium.

Similarly, Dalton does not disclose or suggest

means to ***divide the circuit representation into a plurality of circuit segments***, at least one of the circuit segments containing a plurality of logic gates;

means to allocate a circuit segment identifier ***to each circuit segment***, each circuit segment identifier having circuit segment data associated therewith;

the associative memory mechanism comprising a segment table for storage of segment identifiers and segment data;

means to identify segments that have a state S0 in any one time interval based on the segment data; and

means to retrieve ***only those segments with a state S0, one at a time***, from external memory for evaluation by the associative memory mechanism and means to evaluate the segments with a state S0 in the associative memory mechanism and means to store the result of the evaluation on the ~~active~~ segments in a tangible medium.

MPEP § 2131 notes that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also MPEP § 2131.02. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Because Dalton does not disclose or suggest all of the features recited in claims 66 and 101, Dalton does not anticipate the invention recited in claims 66 and 101, and all claims depending therefrom.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Michael E. Monaco, Reg. No. 52041, at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.147; particularly, extension of time fees.

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Respectfully submitted,

By _____
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